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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,649	04/14/2004	Takashi Kurihara	1076.1094	4917

21171 7590 03/28/2007

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EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,649	KURIHARA ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,21 and 24* is/are pending in the application.

4a) Of the above claim(s) *12-20,22,23, and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,21 and 24* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/823,649 filed on 04/14/2004 and Response to Election/Restriction filed on 02/23/2007. Claims 1-15 and 20-25 are pending.

Claims 1-11, 21, and 24 are elected without traverse.

Claims 12-15, 20, 22, 23, and 25 have been withdraw from consideration. However, Applicant is advised to cancel these claims (non-elected) in the next communication. Claims 1-11, 21, and 24 remain pending in this office action.

Claim Objections

2. Claims 1, 7-9, 11, 21, and 24 are objected to because of the following informalities:

As per claims 1, 1, 21, and 24 recite, "calculating current values of the power supply pad from the current values between the nodes". This limitation appears two different current values: "current value of the power supply pad" and "the current value between the nodes" (which is from the prior step), but do not have a relationship in the functional/structural between the two different current values.

As per claims 1, 7-9, 11, 21, and 24, recite, "adding or eliminating at least power supply pads in accordance with the result of the determination". According to the Application Disclosure there has two different processes corresponding to two different conditions:

i) firstly, eliminating at least one of power supply pad or assigning another type of pad, when the current value of each of the power pads less than the predetermined current capacity; and

ii) secondly, adding at least one of power supply pad when the current value of each of the power pads less than the predetermined current capacity.

Hence, the phrase "adding or eliminating at least one power supply pad" can not be used when only one condition. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8, 11-13, and 20-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Buffet et al. ("Buffet") (US Patent 6,523,150) (see entire document).

5. With respect to claims 1, 11, 21, and 24, Buffet discloses a method, an apparatus, and a recording medium comprising computer instructions stored thereon for determining quantity and positions of a plurality of power supply pads (fig. 1, chip pad region [120] contains plurality of chip pads [125]) in a semiconductor integrated circuit (fig. 1, integrated circuit chip [105]) including a core section (fig. 1, voltage island [130]) provided with a plurality of nodes (fig. 1, see connections [135]), each power supply pad

being connected to the core section via an IO buffer (resistor or RLC) (fig. 1, connections [135] and figs. 6, 7, 9, 10 and 13 with their descriptions), wherein each IO buffer has a predetermined current capacity (the voltage drop in chip voltage island is computed across Vdd, Vddx, and GND based upon the peak or average current and number of chip voltage island pads devoted to power distribution using the chip voltage island model to determine if voltage drop computed is acceptable by comparison to an voltage drop limit determined by the chip designer) (Abstract, fig. 1, fig. 4, steps [190] – [200], col. 5, line 63 – col. 6, line 3, and fig. 5, see the descriptions), the method, the apparatus, and the computer instructions when executed by a computer performing steps including:

(Claim 21) storage device which stores power consumption information of the core section and power supply wire resistance information, including resistances between the nodes (fig. 16); and

(Claim 21) a data processor in communication with the storage device, in which the data processor (fig. 16);

(Claims 1, 21, and 24) performing a power supply network analysis of the core section based on power consumption information the core section and power supply wire resistance information, which includes resistances between the nodes (fig. 1 and fig. 3, col. 4, line 66 – col. 5, line 28 and figs. 6, 7, 9, 10 and 13 with their descriptions);

(Claims 1, 21, and 24) calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes (fig.4, step [190],

col. 5, ll. 35-45, fig. 6, col. 6, line 22 – col. 7, line 5 and figs. 7, 9, 10 and 13 with their descriptions);

(Claims 1, 21, and 24) calculating current values of the power supply pads from the current values between the nodes (fig.4, steps [190]-[200], fig. 5, col. 6, line 13-23, fig. 6, col. 6, line 22 – col. 7, line 5, and figs. 7, 9, 10 and 13 with their descriptions);

(Claims 1, 21, and 24) determining whether the current value of each of the power supply pads exceeds the current capacity the associated IO buffer (if the voltage drop or IR drop is not acceptable) ([fig. 4, step [205], col. 6, ll. 1-5, fig. 5, col. 6, ll. 13-23); and

(Claims 1, 21, and 24) eliminating or adding at least one power supply pad in accordance with the result of the determination (fig. 4, step [210], fig. 11, steps [355] and [360], col. 6, ll. 1-25 and fig. 7 and fig. 8, see the descriptions).

6. With respect to claim 2, Buffet discloses the method according to claim 1, wherein said calculating voltage values of the nodes includes calculating IR drop values between the nodes based on the voltage value each node and suspending subsequent processing when any one of the calculated IR drop values exceeds a predetermined maximum IR drop value (fig.4, step [200] and step [205], fig. 5, and col. 5, line 63 – col. 6, line 22).

7. With respect to claim 3, Buffet discloses the method according to claim wherein said performing a power supply network analysis includes modeling the core section as a plurality of equivalent circuits electrically equivalent to one another (fig. 4, step [195]), each equivalent circuit including a resistor and a current source (fig. 6, col. 6, line 22 –

col. 7, line 5, and fig. 9, col. 7, line 51 – col. 8, line 4) and performing the power supply network analysis on the modeled core section (figs. 6, 7, 9, 10 and 13 with their descriptions)

8. With respect to claim 4, Buffet discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power supply wire density the core section (fig. 8, box [280], col. 7, ll. 15-24 and figs. 6, 7, and 9, see the descriptions).

9. With respect to claim 5, Buffet discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power consumption of the core section (fig. 4, step [195], col. 5, ll. 37-62).

10. With respect to claim 6, Buffet discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of the current values of the power supply pads (fig. 8, box [285], col. 7, ll. 25-38 and figs. 6, 7, and 9, see the descriptions).

11. With respect to claim 7, Buffet discloses the method according to claim 1, wherein the designed semiconductor integrated circuit is provided with a plurality of pads including the power supply pads (fig. 1, and the description), the method further comprising: pads as power supply pads at which the potential is the same (fig. 14 B, col. 9, ll. 34-52), wherein said eliminating or adding at least one power supply pad includes eliminating a power supply pad of which current value is less than the current capacity

(voltage drop or IR drop / power noise is not acceptable) (fig. 4 and figs. 9-14, particular as fig. 11, col. 8 line 35 – col. 9, line 10).

12. With respect to claim 8, Buffet discloses the method according to claim 7, further comprising: determining whether a completion condition is satisfied after deleting the at least one power supply pad, wherein subsequent processing is terminated when the completion condition is satisfied, and said performing a power supply network analysis is executed again when the completion condition is not satisfied (fig. 4, loop [195] – [210], fig. 8 and fig. 11 as first loop and second loop and see the descriptions).

13. With respect to claim 11, Buffet discloses a method provisionally determining quantity and positions of a plurality of power supply pads (fig. 1, chip pad region [120] contains plurality of chip pads [125] and/or [150]) before detailed design of a semiconductor integrated circuit (fig. 1, integrated circuit chip [105] and/or [110]), wherein the semiconductor integrated circuit includes a core section (fig. 1, voltage island [130] and/or [105]) provided with a plurality of nodes (fig. 1, see connections [135] and/or [125A] and [150A]) and a plurality of power supply pads (fig. 1, [125] and/or [150]) , the method comprising:

initially defining all of the pads as power supply pads at which the potential is the same (fig. 14 B, col. 9, ll. 34-52);

performing a power supply network analysis of the core section based on power consumption information the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes

(fig. 1 and fig. 3, col. 4, line 66 – col. 5, line 28 and figs. 6, 7, 9, 10 and 13 with their descriptions);

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes fig.4, step [190], col. 5, ll. 35-45, fig. 6, col. 6, line 22 – col. 7, line 5 and figs. 7, 9, 10 and 13 with their descriptions);

calculating current values of the power supply pads from the current values between the nodes (fig.4, steps [190]-[200], fig. 5, col. 6, line 13-23, fig. 6, col. 6, line 22 – col. 7, line 5, and figs. 7, 9, 10 and 13 with their descriptions);

determining whether there is a power supply pad for which current value is less than or equal to a predetermined current capacity (if the voltage drop or IR drop is not acceptable) ([fig. 4, step [205], col. 6, ll. 1-5, fig. 5, col. 6, ll. 13-23); and

adding a new power supply pad near a power supply pad for which current value exceeds the predetermined current capacity (fig. 4, step [210], fig. 11, steps [355] and [360], col. 6, ll. 1-25 and fig. 7 and fig. 8, see the descriptions), and assigning a power supply pad as another type pad (package pad) (fig. 1, [150], and fig. 9 and fig. 14, see the descriptions) when the current value of that power supply pad is less than or equal to the predetermined current capacity (fig. 4 and figs. 9-14, particular as fig. 11, col. 8 line 35 – col. 9, line 10).

Allowable Subject Matter

14. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if claim 9 is rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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